

## IN THE CLAIMS

1. (Currently amended) A method for testing a cascode circuit comprising an electronic element to be protected from high voltage and a cascode element connected to said electronic element, the method comprising the steps of:

\_\_\_\_\_ arranging a test node between said electronic element and said cascode element;

\_\_\_\_\_ allocating a switching element to said test node and connecting said switching element to said test node, said switching element having a plurality of switching states and being constituted such that its switching state is changed when the voltage at said test node exceeds or falls below a given voltage limit;

\_\_\_\_\_ activating said cascode element using an activation circuit; and

\_\_\_\_\_ detecting the switching state of said switching element using a detection circuit;

wherein said cascode circuit comprises a plurality of electronic elements to be protected from high voltage and a plurality of cascode elements, each cascode element being connected to an electronic element, and wherein a group of switching elements is connected by at least one test line so that the electric signal on said at least one test line indicates whether the switching state of at least one switching element from said group of switching elements is in a changed switching state.

2. (Currently amended) The method according to claim 1, wherein said voltage limit is either chosen to be an upper voltage limit applicable to said electronic element if said electronic element is connected to a ground-voltage line, or is chosen to be a supply voltage minus an upper voltage limit applicable to said electronic element if said electronic element is connected to a supply-voltage line.

3. (Previously presented) The method according to claim 1, wherein said switching element is chosen to comprise a test transistor, preferably an MOS field effect transistor, a gate of said test transistor is connected to said test node, a source of said test transistor is connected to a first test point and a drain of said test transistor is connected to a second test point, a first voltage is applied to said first test point and a second, different voltage is applied to said second test point, and a current flow is detected between said first and said second test point.

4. (Previously presented) The method according to claim 3, wherein said detection of a current flow is used for testing a correct or an incorrect working of said cascode circuit, or for determining a voltage on said test node.

5. (Previously presented) The method according to claim 3, wherein said first voltage is either chosen to be an upper voltage limit applicable to said electronic element if said electronic element is connected to a ground-voltage line, or is chosen to be a supply voltage minus an upper voltage limit applicable to said electronic element if said electronic element is connected to a supply-voltage line, and, in both cases, said second voltage is chosen to slightly differ, e.g., by 1 to 15%, from said first voltage.

6. (Previously presented) The method according to claim 1, wherein said electronic element comprises an MOS field effect transistor of a first channel conduction type, and said test transistor is chosen to be an MOS field effect transistor of the same first channel

conduction type.

7. (Canceled)

8. (Currently amended) The method according to claim 3~~1~~, wherein all sources of said group of test transistors are connected to said first test point and all drains of said group of test transistors are connected to said second test point.

9. (Currently amended) The method according to claim 7~~1~~, wherein each cascode element is consecutively activated.

10. (Currently amended) A cascode circuit comprising:

\_\_\_\_\_ an electronic element to be protected from high voltage;<sub>i</sub>

\_\_\_\_\_ a cascode element connected to said electronic element;<sub>i</sub>

\_\_\_\_\_ a test node arranged between said electronic element and said cascode element;<sub>i</sub>

\_\_\_\_\_ a switching element allocated to said test node and connected to said test node, said switching element having a plurality of switching states and being constituted such that its switching state is changed when the voltage at said test node exceeds or falls below a given voltage limit;<sub>i</sub> and

\_\_\_\_\_ means for detecting the switching state of said switching element;<sub>i</sub>

wherein said cascode circuit comprises a plurality of electronic elements to be protected from high voltage and a plurality of cascode elements, each cascode element being connected to an electronic element, and wherein a group of switching elements is

connected by at least one test line so that the electric signal on said at least one test line indicates whether the switching state of at least one switching element from said group of switching elements is in a changed switching state.

11. (Previously presented) The cascode circuit according to claim 10, wherein said switching element comprises a test transistor, preferably a MOS field effect transistor, a gate of said test transistor being connected to said test node, a source of said test transistor being connected to a first test point and a drain of said test transistor being connected to a second test point, the cascode circuit further comprises means for applying a first voltage to said first test point and means for applying a second, different voltage to said second test point, and means for detecting a current flow between said first and said second test point.

12. (Previously presented) The cascode circuit according to claim 10, wherein said electronic element comprises an MOS field effect transistor of a first channel conduction type, and said test transistor is an MOS field effect transistor of the same first channel conduction type.

13. (Canceled)

14. (Previously presented) The cascode circuit according to claim 11, wherein all sources of said group of test transistors are connected to said first test point and all drains of said group of test transistors are connected to said second test point.